Claims 1-24 are now pending in this application. Claims 6-9 are withdrawn from consideration. Claims 1-5 and 10-24 stand rejected.

In accordance with 37 C.F.R. 1.136(a), a two-month extension of time is submitted herewith to extend the due date of the response to the Office Action dated October 23, 2002, for the above-identified patent application from January 23, 2003, through and including March 23, 2003. In accordance with 37 C.F.R. 1.17(a)(2), authorization to charge a deposit account in the amount of $410.00 to cover this extension of time request also is submitted herewith.

The rejection of Claims 1-3 under 35 U.S.C. § 103 as being unpatentable over McCartney (6,380,801) in view of Fujii et al. (5,184,199) is respectfully traversed.

McCartney describes an operational amplifier (100) that includes an input chop circuit (102) having a pair of input terminals (104, 106) and a pair of output terminals (108, 110). The output terminals are connected to two differential input stages (112, 114) wherein input stage (112) includes a pair of PMOS transistors and input stage (114) includes a pair of transistors that are complementary to input stage (114) transistors for example NMOS transistors. McCartney also describes that the operational amplifier includes an inverter (132) for inverting a signal received from a flip-flop (122).

Fujii et al. describe an inversion mode n-channel MOSFET that includes a silicon single-crystal substrate (1), a β-type silicon carbide single crystal layer (2), an aluminum nitride single-crystal layer (3) that functions as an electrical insulator, and a boron-doped high resistive β-type silicon carbide single-crystal layer (4). Fujii et al. also describe that forming the β-type silicon carbide single crystal layer on the aluminum nitride layer facilitates reducing defects in the β-type silicon carbide single crystal layer because of similarities between β-type silicon carbide single crystal structure and the aluminum nitride layer crystal structure.

Applicants respectfully submit that the Section 103 rejection of the presently pending claims is not a proper rejection. Obviousness cannot be established by merely suggesting that it would have been an obvious to one of ordinary skill in the art to modify McCartney according to the teachings of Fujii et al. More specifically, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. Neither McCartney nor Fujii et al., considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to combine McCartney with Fujii et al. because there is no motivation to combine the references suggested in the art. Rather, the Examiner has not pointed to any prior art that teaches or suggests to combine the disclosures, other than Applicants' own teaching. Only the conclusory statement that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace the nmos transistors of McCartney with the silicon carbide nmos depletion transistors so as to enable operation under severe conditions as taught by Fujii et al." suggests combining the disclosures.

Furthermore, Applicants respectfully submit that the prior art teaches away from each other. More specifically, at column 1, line 51 through line 54 McCartney describes that the basic idea is "to provide for the lower part of the input voltage range with the PMOS stage 12 and the upper part of the input range with the NMOS stage 14" However, in contrast to McCartney, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer. Accordingly, Applicants respectfully submit McCartney teaches away from Fujii et al., and as such, there is no suggestion or motivation to combine McCartney with Fujii et al.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there

must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion nor motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Although it is asserted within the Office Action that McCartney teaches the present invention except for disclosing the silicon carbide nmos depletion transistors, and that Fujii et al. discloses silicon carbide nmos depletion transistors, no motivation nor suggestion to combine the prior art disclosures has been shown. Since there is no teaching nor suggestion in the cited art for the claimed combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicants request that the Section 103 rejection of Claims 1-3 be withdrawn.

Further, and to the extent understood, neither McCartney nor Fujii et al., considered alone or in combination, describe or suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited combination. Specifically, Claim 1 recites a method for amplifying a signal including "generating an input signal; and amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate." Neither McCartney nor Fujii et al., considered alone or in combination, describe or suggest a method for amplifying a signal including generating an input signal, and amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the

first stage and the second stage fabricated on the same silicon carbide substrate. Moreover, neither McCartney nor Fujii et al., considered alone or in combination, describe a method that includes "amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate." Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages wherein the second input stage includes a pair of transistors that are complementary to the first input stage, and Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer. For the reasons set forth above, Claim 1 is submitted to be patentable over McCartney in view of Fujii et al.

Claims 2-3 depend directly from independent Claim 1. When the recitations of Claims 2-3 are considered in combination with the recitations of Claim 1, Applicant respectfully submits that dependent Claims 2-3 likewise are patentable over McCartney in view of Fujii et al.

For the reasons set forth above, Applicant respectfully requests that the rejection of Claims 1-3 under 35 U.S.C. § 103 be withdrawn.

The rejection of Claims 4-5 under 35 U.S.C. § 103 as being unpatentable over McCartney (6,380,801) in view of Fujii et al. (5,184,199) and further in view of Richter et al. (4,647,845) is respectfully traversed.

McCartney and Fujii et al. are described above. Richter et al. describe a sweep oscillator (10) connected to a device under test (14) and a scalar AC network analyzer (22). An AC/DC detector (18) receives an RF signal (28) on a line (16) from the device under test. The detector is capable of operating in an AC detection mode and a DC detection mode. The detector includes an RF detector (40) connected to a chopper (44). The RF detector detects the RF signal and

transforms it into a rectified signal. In the DC detection mode, the chopper modulates the rectified signal to produce a modulated signal. In the AC detection mode, the chopper does not modulate the signal because it is already modulated. The modulated signal is supplied to a preamplifier (48) to generate an amplified signal.

Applicant respectfully submits that the Section 103 rejection of the presently pending claims is not a proper rejection. Obviousness cannot be established by merely suggesting that it would have been obvious to one of ordinary skill in the art to modify McCartney according to the teachings of Fujii et al. and Richter et al. More specifically, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. Rather, the present Section 103 rejection appears to be based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, McCartney is cited for its teaching of an operational amplifier that includes an input chop circuit and two differential input stages wherein the second input stage includes a pair of transistors that are complementary to the first input stage, Fujii et al. is cited for its teaching that a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. are cited for their teaching that a network analyzer that can transform a pulsed RF signal to produce an AC signal. Since there is no teaching nor suggestion in the cited art for the claimed combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicant respectfully requests that the Section 103 rejection be withdrawn.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there

must be some suggestion, outside of Applicant's disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Applicant respectfully submits that a closer examination of the prior art would reveal that the prior art teaches away from the present invention. More specifically, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited art. Specifically, Claims 4 and 5 depend either, directly or indirectly, from independent Claim 1 which recites a method for amplifying a signal including "generating an input signal; and amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate." None of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest a method for amplifying a signal including generating an input signal, and amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second stage fabricated on a silicon carbide substrate. Moreover, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe a method that includes "amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier, wherein the operational amplifier includes a first NMOS depletion mode amplification stage and a second NMOS depletion mode amplification stage, the first stage and the second

stage fabricated on the same silicon carbide substrate." Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages wherein the second input stage includes a pair of transistors that are complementary to the first input stage, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. describe a network analyzer that can transform a pulsed RF signal to produce an AC signal. For the reasons set forth above, Claim 1 is submitted to be patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claims 4-5 depend directly from independent Claim 1. When the recitations of Claims 4-5 are considered in combination with the recitations of Claim 1, Applicant respectfully submits that dependent Claims 4-5 likewise are patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

For the reasons set forth above, Applicant respectfully requests that the rejection of Claims 4-5 under 35 U.S.C. § 103 be withdrawn.

The rejection of Claims 10 and 14-24 under 35 U.S.C. § 103 as being unpatentable over McCartney (6,380,801) in view of Fujii et al. (5,184,199) and further in view of Richter et al. (4,647,845) is respectfully traversed.

McCartney, Fujii et al., and Richter et al. are described above. Applicant respectfully submits that the Section 103 rejection of the presently pending claims is not a proper rejection. Obviousness cannot be established by merely suggesting that it would have been obvious to one of ordinary skill in the art to modify McCartney according to the teachings of Fujii et al. and Richter et al. More specifically, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. Rather, the present Section 103 rejection

appears to be based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, McCartney is cited for its teaching of an operational amplifier that includes an input chop circuit and two differential input stages wherein the second input stage includes a pair of transistors that are complementary to the first input stage, Fujii et al. is cited for its teaching that a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. is cited for its teaching that a network analyzer that can transform a pulsed RF signal to produce an AC signal. Since there is no teaching nor suggestion in the cited art for the claimed combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicant respectfully requests that the Section 103 rejection be withdrawn.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicant's disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Applicant respectfully submits that a closer examination of the prior art would reveal that the prior art teaches away from the present invention. More specifically, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited art. Specifically, Claim 10 recites an operational amplifier circuit including "a first NMOS depletion mode amplification stage; a first NMOS depletion mode chopping switch

responsive to a first chopping signal to chop an input signal to said first amplification stage; a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a voltage dropping element." None of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from the first amplification stage, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a voltage dropping element. Moreover, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch, a second NMOS depletion mode chopping switch, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit. Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages, wherein the first input stage includes a pair of PMOS transistors and the second input stage includes a pair of NMOS, McCartney does not describe or suggest a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch, a second NMOS depletion mode chopping switch, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit. Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. describe a network analyzer that can transform a pulsed RF signal to produce an AC signal. For the reasons set forth above, Claim 10 is

submitted to be patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claim 14 recites an operational amplifier circuit including "a first NMOS depletion mode amplification stage; a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage; a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a resistor; and further wherein said first NMOS depletion mode amplification stage, said first NMOS depletion mode chopping switch, said second NMOS depletion mode chopping switch, and said NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit are fabricated on the same silicon carbide substrate."

None of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from the first amplification stage, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a resistor, and further wherein the first NMOS depletion mode amplification stage, the first NMOS depletion mode chopping switch, the second NMOS depletion mode chopping switch, and the NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit are fabricated on the same silicon carbide substrate. Moreover, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest an operational amplifier including an a first NMOS

depletion mode amplification stage, a first NMOS depletion mode chopping switch, a second NMOS depletion mode chopping switch, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit fabricated on the same silicon carbide substrate. Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages wherein the first input stage includes a pair of PMOS transistors and the second input stage includes a pair of NMOS, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. describe a network analyzer that can transform a pulsed RF signal to produce an AC signal. For the reasons set forth above, Claim 14 is submitted to be patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claims 15-16 depend directly from independent Claim 14. When the recitations of Claims 15-16 are considered in combination with the recitations of Claim 14, Applicant respectfully submits that dependent Claims 15-16 likewise are patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claim 17 recites an operational amplifier circuit including "a first NMOS depletion mode amplification stage having differential inputs and outputs; a first NMOS depletion mode chopping switch responsive to a first chopping signal and a second chopping signal to chop a differential input signal to said first amplification stage; a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal and a level shifted second chopping signal to chop an output signal from said first amplification stage; a first NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a first resistor; a second NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to said clock signal to generate

said second chopping signal and said level shifted second chopping signal across a second resistor; and a clock generator circuit configured to generate said clock signal."

None of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest an operational amplifier circuit including a first NMOS depletion mode amplification stage having differential inputs and outputs, a first NMOS depletion mode chopping switch responsive to a first chopping signal and a second chopping signal to chop a differential input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal and a level shifted second chopping signal to chop an output signal from the first amplification stage, a first NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a first resistor, a second NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to the clock signal to generate the second chopping signal and the level shifted second chopping signal across a second resistor, and a clock generator circuit configured to generate the clock signal. Moreover, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch, a second NMOS depletion mode chopping switch, and a level shifted second chopping signal to chop an output signal from the first amplification stage. Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages wherein the first input stage includes a pair of PMOS transistors and the second input stage includes a pair of NMOS, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. describe a network analyzer that can transform a pulsed RF signal to produce an AC signal.

For the reasons set forth above, Claim 17 is submitted to be patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claims 18-21 depend either, directly or indirectly, from independent Claim 17. When the recitations of Claims 18-21 are considered in combination with the recitations of Claim 17, Applicant respectfully submits that dependent Claims 18-21 likewise are patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claim 22 recites a method for amplifying a signal including "generating an input signal; amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal; amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal; and amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage to produce an amplified chopped output signal."

None of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe or suggest a method for amplifying a signal including generating an input signal, amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal, and amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage to produce an amplified chopped output signal. Moreover, none of McCartney, Fujii et al., and Richter et al., considered alone or in combination, describe nor suggest "amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier and amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch." Rather, in contrast to the present invention, McCartney describes an operational

amplifier that includes an input chop circuit and two differential input stages wherein the first input stage includes a pair of PMOS transistors and the second input stage includes a pair of NMOS, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, and Richter et al. describe a network analyzer that can transform a pulsed RF signal to produce an AC signal. For the reasons set forth above, Claim 22 is submitted to be patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

Claims 23-24 depend either, directly or indirectly, from independent Claim 22. When the recitations of Claims 23-24 are considered in combination with the recitations of Claim 22, Applicant respectfully submits that dependent Claims 23-24 likewise are patentable over McCartney in view of Fujii et al. and further in view of Richter et al.

For the reasons set forth above, Applicant respectfully requests that the rejection of Claims 10, and 14-24 under 35 U.S.C. § 103 be withdrawn.

The rejection of Claims 11-13 under 35 U.S.C. § 103 as being unpatentable over McCartney (6,380,801) in view of Fujii et al. (5,184,199), Richter et al. (4,647,845) and further in view of White et al. (4,558,235) is respectfully traversed.

McCartney, Fujii et al., and Richter et al. are described above. White et al. describe a gallium arsenide logic gate which couples a logic switch node to an output node both through a voltage level shifter circuit, for DC coupling, and a feed-forward capacitor, for AC coupling. White et al. also describe that a forward-biased Schottky diode is preferably used for voltage shifting.

Applicant respectfully submits that the Section 103 rejection of the presently pending claims is not a proper rejection. Obviousness cannot be established by merely suggesting that it would have been obvious to one of ordinary skill in the art to modify McCartney according to

the teachings of Fujii et al., Richter et al., and White et al. More specifically, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. Rather, the present Section 103 rejection appears to be based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, McCartney is cited for its teaching of an operational amplifier that includes an input chop circuit and two differential input stages wherein the second input stage includes a pair of transistors that are complementary to the first input stage, Fujii et al. is cited for its teaching that a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer facilitates reducing defects in the β-type silicon carbide single crystal layer, Richter et al. is cited for its teaching that a network analyzer that can transform a pulsed RF signal to produce an AC signal, and White et al. is cited for its teaching that a forward-biased Schottky diode can be used for voltage shifting. Since there is no teaching nor suggestion in the cited art for the claimed combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicant respectfully requests that the Section 103 rejection be withdrawn.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicant's disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Applicant respectfully submits that a closer examination of the prior art would reveal that the prior art teaches away from the present invention. More specifically, none of McCartney, Fujii et al., Richter et al., and White et al., considered alone or in combination, describe or suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited art. Specifically, Claims 11-13 depend either, directly or indirectly, from independent Claim 10 which recites an operational amplifier circuit including "a first NMOS depletion mode amplification stage; a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage; a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a voltage dropping element." None of McCartney, Fujii et al., Richter et al., and White et al., considered alone or in combination, describe or suggest an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a voltage dropping element. Moreover, none of McCartney, Fujii et al., Richter et al., and White et al., considered alone or in combination, describe an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch, a second NMOS depletion mode chopping switch, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit. Rather, in contrast to the present invention, McCartney describes an operational amplifier that includes an input chop circuit and two differential input stages wherein the first input stage includes a pair of PMOS transistors and

the second input stage includes a pair of NMOS, Fujii et al. describe a β-type silicon carbide single crystal layer fabricated on an aluminum nitride layer that facilitates reducing defects in the β-type silicon carbide single crystal layer, Richter et al. describes a network analyzer that can transform a pulsed RF signal to produce an AC signal, and White et al. describe that a forward-biased Schottky diode is preferably used for voltage shifting. For the reasons set forth above, Claim 10 is submitted to be patentable over McCartney in view of Fujii et al., Richter et al., and further in view of White et al.

Claims 11-13 depend either, directly or indirectly, from independent Claim 10. When the recitations of Claims 11-13 are considered in combination with the recitations of Claim 10, Applicant respectfully submits that dependent Claims 11-13 likewise are patentable over McCartney in view of Fujii et al., Richter et al., and further in view of White et al.

For the reasons set forth above, Applicant respectfully requests that the rejection of Claims 11-13 under 35 U.S.C. § 103 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Donald Thomas McGrath

Serial No.: 09/682,863

Filed: October 25, 2001

For: METHODS AND APPARATUS FOR AMPLIFICATION IN HIGH TEMPERATURE ENVIRONMENTS

Art Unit: 2817

Examiner: Shingleton, Michael B.

SUBMISSION OF MARKED UP CLAIMS

Box: RCE
Hon. Commissioner for Patents
Washington, D.C. 20231

Submitted herewith are marked up Claims in accordance with 37 C.F.R. 1.121(c)(1)(ii), wherein additions are underlined and deletions are [bracketed].

IN THE CLAIMS

1. (once amended) A method for amplifying a signal comprising:

generating an input signal; and

amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, the operational amplifier including a first NMOS depletion mode amplification stage and a second NMOS

depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate.

14. (once amended) An operational amplifier circuit comprising:

a first NMOS depletion mode amplification stage;

a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage;

a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and

and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a resistor;

and further wherein said first NMOS depletion mode amplification stage, first NMOS depletion mode chopping switch, second NMOS depletion mode chopping switch, and said NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit are [operational amplifier circuit is] fabricated on [a] the same silicon carbide substrate.

Respectfully Submitted,

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